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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/666,277	09/21/2000	David William Boerstler	AUS9-2000-0240-US1	8443

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2634	6

DATE MAILED: 06/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/666,277	BOERSTLER, DAVID WILLIAM	
	Examiner	Art Unit	
	Sudhanshu C. Pathak	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *April 2nd, 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *47-50* is/are allowed.

6)☒ Claim(s) *1-4,7,10,12 and 35-37* is/are rejected.

7)☒ Claim(s) *5,6,8,9,11,13-34 and 38-46* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *September 21st, 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-to-50 are pending in the application.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3 & 7, are rejected under 35 U.S.C. 102(b) as being anticipated by Van Driest et al. (5,003,562).

Regarding to Claim 1, Van Driest discloses a decoder for use in decoding self-clocked transmission system (Abstract, lines 1-4 & Column 1, lines 10-16). Van Driest further discloses the decoder (Fig. 3A & Fig. 3B) comprising a first and second monostable circuit (Fig. 3B, elements 70 & 74), and comparator logic circuit (Fig. 3B, element 86 & Fig. 7). Van Driest further discloses inputting the received data signal (Fig. 3A, element 40, "RD") to both first and second monostable circuits (Column 3, lines 47-52) and generating a first and second output signals (Fig. 3B, elements 80 & 82) and further comparing the output signals of the monostable circuits (Figure 3B, elements 80, 82 & 86) and outputting a compared output signal based on the comparison (Column 7, lines 23-46).

Regarding to Claim 2, Van Driest discloses a decoder for use in decoding self-clocked transmission system as described above. Van Driest further discloses the signal recovery decoder to consist of at least one clock signal (Fig. 2, element 18 &

Fig. 3A, element 72 & 76) and a data signal (Fig. 2, element 18 & Fig. 3A, element 40).

Regarding to Claim 3, Van Driest discloses a decoder for use in decoding self-clocked transmission system as described above. Van Driest further discloses the received data signal to be at least one of processed equalized data signal and a processed unequalized data signal (Fig. 3A, element 40). Furthermore, Van Driest discloses that the transmitted signal, which is received by the decoder, is distorted and noise signals are introduced resulting in jitter (Column 2, lines 53-63).

Regarding to Claim 7, Van Driest discloses a decoder for use in decoding self-clocked transmission system as described above. Van Driest further discloses the decoder (Fig. 3A & Fig. 3B) comprising a first and second monostable circuit (Fig. 3B, elements 70 & 74), and furthermore the monostable circuits to comprise a data flip-flop, which is a one-shot, circuit component.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Van Driest et al. (5,003,562) in view of Kobayashi (6,028,461).

Regarding to Claim 4, Van Driest discloses a decoder for use in decoding self-clocked transmission system as described above. However, Van Driest does not

disclose the comparator logic circuit (Fig. 3B, element 86 & Fig. 7) to include an OR-gate.

Kobayashi discloses a clock adjusting circuit comprising multiple phase comparison circuits to detect the difference between a reference clock and a loopback signal of the clock output (Abstract, lines 1-6). Furthermore, Kobayashi discloses the phase comparison circuit to include an OR-gate (Fig. 2, element 136). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the comparator logical circuit as described in Kobayashi in the phase comparator logic in the decoder as described in Van Driest.

5. Claims 10, 35 & 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Driest et al. (5,003,562) in view of Park (5,880,898).

Regarding to Claim 10, Van Driest discloses a decoder for use in decoding self-clocked transmission system as described above. However, Van Driest does not disclose an equalizer to equalize the received input data signal.

Park discloses a circuit to equalize or remove error signals in digital data signals (Abstract, lines 6-11). Park discloses the equalizer circuit (Fig. 3, element 100 & Figure 4) to include a differentiator (Fig. 4, element 61) for differentiating the input signal, an amplifier (Fig. 4, elements 62 & 63) for amplifying the differentiated data, a sign element (Fig. 4, element 70) to apply a sign to the amplified data. The signed amplified data signal is decreased due to the attenuation and coupling of the signals in the transmission lines. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the equalizer as described in

Park to the decoder circuit as described in Van Driest so as to remove any glitches or distortions in the received data so as to accurately then decode the data signals.

Regarding to Claim 35, Van Driest discloses a decoder for use in decoding self-clocked transmission system (Abstract, lines 1-4 & Column 1, lines 10-16). Van Driest further discloses the decoder (Fig. 3A & Fig. 3B) comprising a first and second monostable circuit having at least two input ports and two output ports (Fig. 3B, elements 70 & 74), and comparator logic circuit (Fig. 3B, element 86 & Fig. 7). Van Driest further discloses a compare logic circuitry (Fig. 3B, element 86 & Fig. 7), having at least two input ports and one output port (Fig. 3B, elements 80, 82 & 90), wherein the first output port of the first monostable circuit is connected to the first input of the logic circuitry and the first output of the second monostable circuit is connected to the second input port of the logic circuitry. However, Van Driest does not disclose implementing an equalizer in the decoder circuitry wherein the output of the equalizer is input into the monostable circuit components and does not explicitly disclose at least two output ports in the monostable circuit.

Park discloses a circuit to equalize or remove error signals in digital data signals (Abstract, lines 6-11). Park further discloses the equalizer comprising at least one output port (Fig. 3, element 100 & Fig. 4, element "NON-GLITCH"). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the equalizer as described in Park to the decoder circuit as described in Van Driest so as to remove any glitches or distortions in the received data so as to then decode the data signals and obtain a more accurate clock signal and the

transmitted data. Furthermore, Van Driest implements the monostable circuits using "D" Flip-Flops, which comprises two output ports.

Regarding to Claim 36, Van Driest in view of Park discloses a decoder for use in decoding self-clocked transmission system as described above. However, Van Driest in view of Park does not disclose a data flip-flop circuit component having a data input port, a clock input port and a complementary clock input port and having an output port and a complementary output port.

The Examiner takes official notice that a positive edge-triggered "D" flip-flop provides a data input port and a clock input port and a negative edge-triggered "D" flip-flop provides a data input port and a complementary clock input port. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that implementing a combination of a negative and positive edge-triggered flip-flop circuits wherein a constant signal is connected to the complementary clock input port of the data flip-flop satisfies the limitations of the claim.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Van Driest et al. (5,003,562) in view of Park (5,880,898) in further view of Streckmann et al. (4,535,299).

Regarding to Claim 12, Van Driest in view of Park discloses a decoder for use in decoding self-clocked transmission system as described above. Park further discloses that an optimum differentiation width can be set by varying the time constant to remove a glitch than the data (Column 4, lines 12-15). However Van

Driest in view of Park does not disclose the differentiator to as a resistive-capacitive differentiator.

Streckmann discloses a resistive-capacitive differentiator (Fig. 1, elements C1 & R1), for differentiating the incoming signal (Column 3, lines 57-63). Furthermore, Streckmann discloses varying the values of the resistor and /or the capacitor so as to obtain the optimum time constant for the frequency of the incoming signal (Column 3, lines 57-67 & Column 4, lines 15-27). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that by implementing the differentiator as described in Streckmann in the decoder as described in Van Driest in view of Park the optimum time constant can be achieved by varying the R-C values of the differentiator, and thus provide increased flexibility for the data rate into the equalizer.

7. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Van Driest et al. (5,003,562) in view of Park (5,880,898) in further view of Kobayashi (6,028,461).

Regarding to Claim 37, Van Driest in view of Park discloses a decoder for use in decoding self-clocked transmission system as described above. However, Van Driest in view of Park does not disclose the comparator logic circuit (Fig. 3B, element 86 & Fig. 7) to include an OR-gate.

Kobayashi discloses a clock adjusting circuit comprising multiple phase comparison circuits to detect the difference between a reference clock and a loopback signal of the clock output (Abstract, lines 1-6). Furthermore, Kobayashi

discloses the phase comparison circuit to include an OR-gate (Fig. 2, element 136). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the comparator logical circuit as described in Kobayashi in the phase comparator logic in the decoder as described in Van Driest in view of Park.

Allowable Subject Matter

8. Claims 5, 6, 8, 9, 11, 13-34 & 38-46 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claims 47-50 are allowable over prior art of record because the cited references do not contain the specified limitation of a first and second monostable circuit having an trigger signal input and each having positive and a negative edge output and logical operator having one input to be the negative edged output and the other input to be the positive edged output and further outputting a recovered clock out signal.

Response to Arguments

10. Applicant's arguments filed on April 2nd, 2004 have been fully considered but they are not persuasive. The arguments presented in the Amendment are that a person of ordinary skill in the art would not recognize that a D flip-flop as a monostable circuit component, however Haubner et al. (4,459,591) does indeed disclose a monostable flip-flop (Fig. 5, element 64 & Column 9, lines 10-32). Furthermore, Berney (4,439,717) discloses a D flip-flop operating as a

monostable circuit (Fig. 4, element 12 & Column 4, lines 10-27). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that a D flip-flop can be considered a monostable circuit component thus satisfying the limitations of the claims.

It is recommended to the applicant to consider the detailed list of pertinent references included with this Office Action (See Attached "Notice of References Cited" (PTO-892)), which disclose monostable flip-flops.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sudhanshu C. Pathak whose telephone number is (703) 305-0341. The examiner can normally be reached (Monday-Friday from 8:30 AM to 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin, can be reached at (703) 305-4714.

Any response to this action should be mailed to:

- Commissioner of Patents and Trademarks Washington, D.C. 20231

Or faxed to:

- (703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to:

- Crystal Part II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to:

Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600